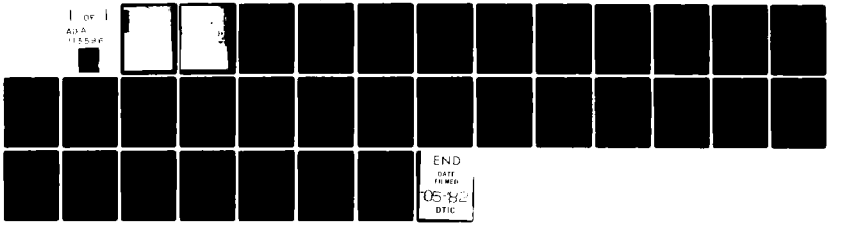
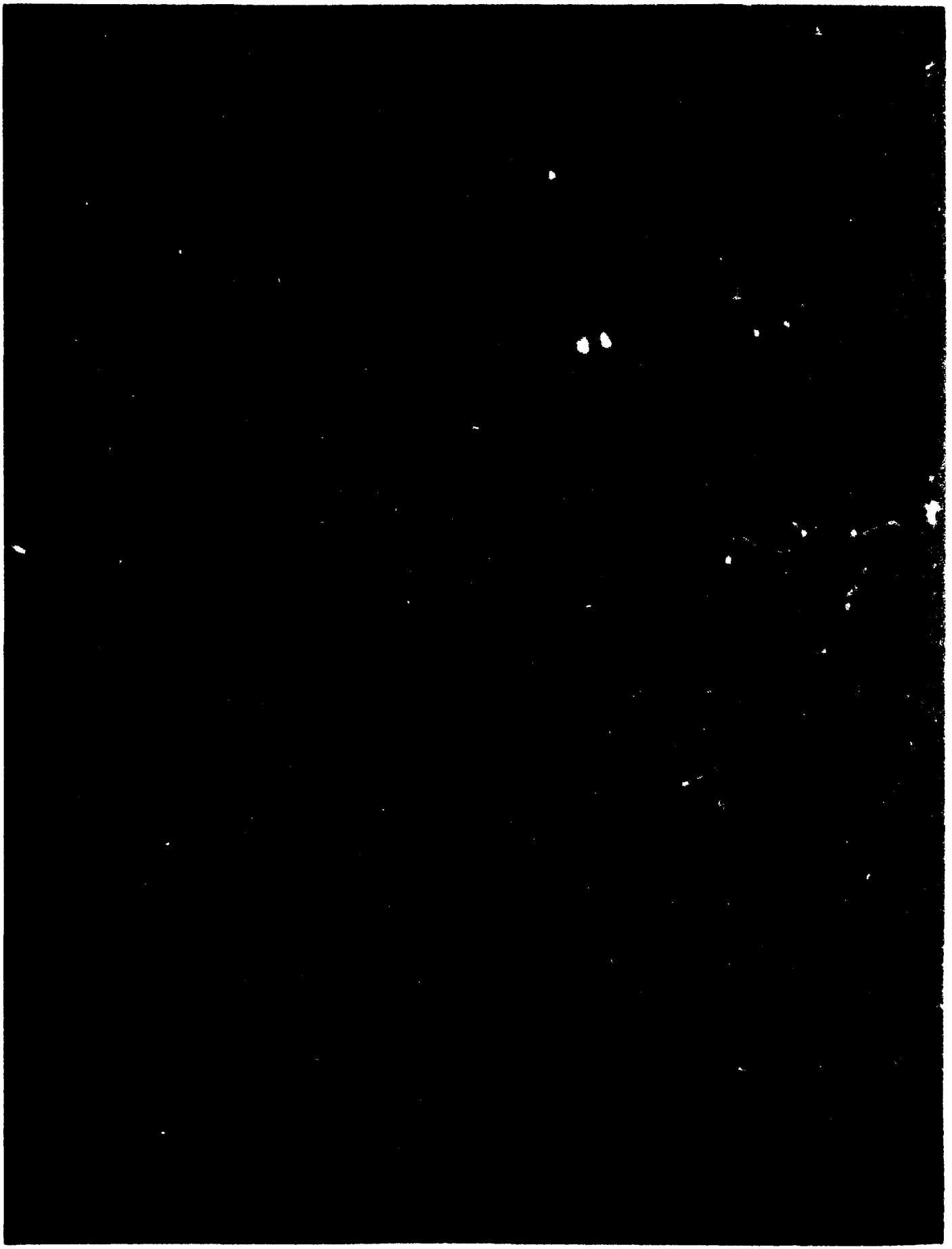
AD-A113 596 HARRY DIAMOND LABS ADELPHI MD F/G 9/2
A NOVEL SCANCONVERTING OSCILLOGRAPHIC TECHNIQUE FOR IN-SITU SIG--ETC(U)
JAN 82 J VANDERWALL, M CONNER
UNCLASSIFIED HDL-TR-1956 NL





UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Date Entered)

REPORT DOCUMENTATION PAGE	READ INSTRUCTIONS BEFORE COMPLETING FORM
1. REPORT NUMBER: HDL-TR-1956	2. GOVT ACCESSION NO.: AD-A113596
3. RECIPIENT'S CATALOG NUMBER	
4. TITLE (and Subtitle): A Novel Scan-Converting Oscillographic Technique for In-Situ Signal Acquisition with Subsequent Automatic Digitization	5. TYPE OF REPORT & PERIOD COVERED: Technical Report
	6. PERFORMING ORG. REPORT NUMBER
7. AUTHOR(s): Jonathan Vanderwall, Michael Conner	8. CONTRACT OR GRANT NUMBER(s)
9. PERFORMING ORGANIZATION NAME AND ADDRESS: Harry Diamond Laboratories, 2800 Powder Mill Road, Adelphi, MD 20783	10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS: Program Ele: 6.26.03.A, DA Project: 1L662626AH18
11. CONTROLLING OFFICE NAME AND ADDRESS: U.S. Army Armament Research and Development Command, Dover, NJ 07801	12. REPORT DATE: January 1982
	13. NUMBER OF PAGES: 35
14. MONITORING AGENCY NAME & ADDRESS(if different from Controlling Office)	15. SECURITY CLASS. (of this report): UNCLASSIFIED
	15a. DECLASSIFICATION/DOWNGRADING SCHEDULE

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

HDL Proj: A18132
DRCMS Code: 612603.H.180111

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Video tape recorder
Scan converter
Transient digitization

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report discusses the development of a novel equipment for the remote acquisition of oscillographic data in the form of a scan-converted television signal, its temporary storage by means of an inexpensive video tape recorder, and its subsequent digitization. The essential feature of this equipment is its property of scan conversion: signals captured by a Tektronix R7912 Transient Digitizer are read out not in digital form, but rather as television images of the acquired traces, recorded at the site of the experiment, and returned to the laboratory for subsequent digitization and processing.

DD FORM 1 JAN 73 1473 EDITION OF 1 NOV 65 IS OBSOLETE

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Date Entered)

CONTENTS

FIGURES

TABLE

1. INTRODUCTION

This report discusses the development of a novel equipment for the remote acquisition of oscillographic data in the form of a scan-converted television signal, its temporary storage by means of an inexpensive video tape recorder (VTR), and its subsequent digitization. The essential feature of this equipment is its property of scan conversion: signals captured by a Tektronix R7912 Transient Digitizer are read out not in digital form but rather as television images of the acquired "traces" recorded at the site of the experiment and returned to the laboratory for subsequent digitization and processing.

The need for such an instrument was engendered by an experiment in aerosol backscattering, which it is pertinent to describe briefly. A gallium arsenide injection laser is excited to produce fast-rising pulses of infrared radiation, 5 to 10 ns wide.[1] Optics exterior to the laser collimate and plane polarize the beam, which is then incident upon the aerosol. Backscattered photons are then incident upon two receivers, one responsive to light polarized in the same sense as the transmitted beam and the other responsive to light polarized at right angles to this. The purpose of the experiment was to investigate the degree to which the backscattered pulse is stretched and depolarized by the aerosol, as providing potential means of discriminating between, say, clouds and the earth.[2,3] Further, there was a need to record the pulse shape to provide experimental verification of the model for the backscattered return, V(t), given by[4]

$$V(t) = K\int_{-\infty}^{\infty} P(t-\tau)C(c\tau/2)R(c\tau/2)\,d\tau$$

where

K = proportionality constant,
P = transmitted power,
$C(x) = \mu(x)e^{2\int_0^x \alpha(s)\,ds}$,
μ = volume backscatter coefficient,
α = extinction coefficient,
c = speed of light,
R = range law.

Several points present themselves immediately. For example, one cannot bring real clouds from the sky into the laboratory for examination: the experiment must go to the clouds—in this case, by helicopter. Thus, the system must be relatively portable. Also, received signals may have rise times shorter than 2 ns so that the instrument used to record them must have an effective bandpass on the order of 250 to 300 MHz. Because the transition from clear air to aerosol is of interest, it is necessary to examine returns obtained at intervals of 30 ms or less so that reasonable forward speeds may be maintained in order that the vortices shed by the main rotor of the helicopter will not induce turbulence in the sample volume. Moreover, it is necessary to take data for relatively lengthy periods: experience has shown that the absolute minimum time required for conducting this experiment is 45 s and even then there is grave risk that vital data will be missed.

Initially, the system used to display and record the returned pulses consisted of a broadband oscilloscope viewed by a motion picture camera. (The laser modulator and the oscilloscope were both synchronized to the opening of the camera shutter.) That system

[1] *J. Vanderwall, W. V. Hattery, and Z. G. Sztankay, Subnanosecond Rise Time Pulses from Injection Lasers, IEEE J. Quantum Electron.*, **QE-10** (July 1974), 570-572.

[2] Z. G. Sztankay and D. W. McGuire, Backscatter in Clouds at 0.9 μm and Its Effect on Optical Fuzing Systems (U), Proceedings of Seventh DoD Conference on Laser Technology (November 1977). (SECRET)

[3] Dennis McGuire, Michael Conner, and Theodore Hopp, Aerosol Discrimination by Electronic High- and Low-Pass Filtering, Harry Diamond Laboratories HDL-TR-1939 (December 1980).

[4] *Dennis McGuire and Michael Conner, The Deconvolution of Aerosol Backscattered Optical Pulses to Obtain System-Independent Aerosol Signatures, Harry Diamond Laboratories HDL-TR-1944 (June 1981).*

proved to have very serious drawbacks. Even the most sensitive recording film, specially processed, did not always yield the desired writing rate. Only a few minutes' worth of film could reasonably be carried and processed. It was not possible to monitor the test in progress or to examine the quality of the data on the spot. In consequence, many opportunities for improvement of the experimental procedure were lost. It was to overcome these objections and to provide automatic digitization that the equipment described in this report was developed.

The digitizing apparatus comprises four major blocks: (1) Tektronix R7912 Transient Digitizer, (2) helical-scan VTR, (3) Video Processor, and (4) Video Digitizer and Computer Interface Unit. Block diagrams of the acquisition-recording and playback-digitizing configurations are given as figures 1 and 2. The function of the R7912 is to capture a fast pulse and to transfer its image in a standard video format to the VTR. The tape recorder is used as an intermediate memory to store the R7912 signals. During the recording of the images, the Video Processor sequentially numbers the frames from 0 to $2^{16} - 1$, and during the playing back of the recorded data it converts the tape recorded signal to signals usable by the digitization section of the equipment. This conversion involves recovery of synchronizing information, recovery of the frame number, and threshold detection of the video signal. The Digitizer/Interface converts the output of the Video Processor into a stream of 8-bit bytes, which are compatible with the memory channel of an Interdata 7/32 computer.

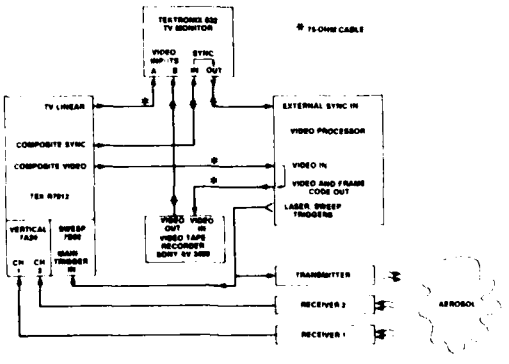


Figure 1. Block diagram of acquisition and recording configuration.

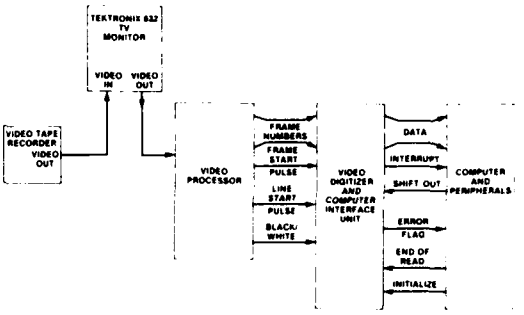


Figure 2. Block diagram of playback and digitizing configuration.

1.1 R7912 Transient Digitizer

The principle underlying the operation of the R7912 is that of scan conversion. The implementation of this concept is interesting: a wideband oscilloscope cathode ray tube (CRT) deflection structure writes not as is customary upon a phosphor screen, but directly upon the target of a vidicon. The target, which is about 1.3 × 0.95 cm, comprises an array of silicon diodes. The diode density is about 800/cm, yielding about 8×10^5 diodes in the target area. Initially, the diodes are all uniformly charged to the same potential by the reading beam. (The reading beam is incident upon the opposite side of the target from the writing beam and has its own deflection structure independent of the writing beam.) Whenever and wherever the writing beam strikes the target, the diodes are discharged to some degree, depending upon the beam current, the spot size, the velocity, and so forth. When the reading beam again traverses these areas, the

[5] *Yoshio Sawaji, EIAJ Standards for 1/2 Inch Videotape Recorders, J. Soc. Motion Pict. Telev. Eng.,* **79** *(December 1970), 1091-1093.*

current required to recharge them may be sensed and amplified. The usual mode of operation is to use the internal digitizing feature of the R7912 in conjunction with a dedicated minicomputer. The refresh rate in this mode is, at best, too low for our application by a factor of four. Furthermore, even if it were made faster, the vast amount of digital data could not economically be stored by any portable means.

We therefore elected to operate the R7912 in its nonstore mode, in which the target is read out in a manner analogous to the operation of a television camera, the output signal being a composite television signal depicting the acquired data as they would appear on the screen of a conventional oscilloscope. Such a signal is amenable to convenient storage by means of a helical-scan VTR, and that is the approach taken here.

It proved necessary to modify the R7912 to reduce the data rate to an acceptable number of bytes per second. The principle of the modification is illustrated in figure 3. In figure 3(a), the written trace is read by a raster scan parallel to the time axis as in the normal mode of operation of the R7912. It is plain that some of the television lines do not cross the trace at all, while others may cross it many times. By rotating the readout scan 90 deg as in figure 3(b), the amount of data per line can be made small and constant. Each time a readout scan line crosses a written trace, there ought, in principle, to be two and only two points of interest—one and only one black-to-white transition and one and only one white-to-black transition (fig. 3c). In principle, it would be possible to change the direction of writing on the scan-converter tube to achieve the same object, as by interchanging the horizontal and vertical plug-ins. The bandwidth of the horizontal channel is only about 2 percent of the vertical bandwidth so that this interchange is not possible. It is, however, quite easy to change the direction of the readout scan by 90 deg. This change is described in appendix A.

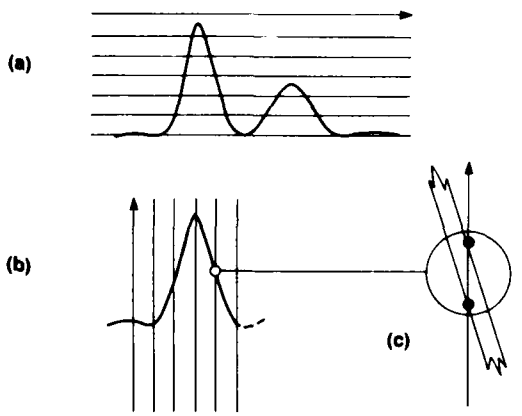


Figure 3. Modification of readout scan to decrease data rate.

1.2 Video Tape Recorder

The VTR used is a SONY AV-3400, although any helical-scan VTR conforming to Electronic Industries Association EIAJ type 1 standards[5] could have served. (Indeed, a broadcast-standard quadruplex recorder could be used, but only with substantial penalties in weight, size, power consumption, tape consumption, and acquisition cost.) The machine in question is a monochrome recorder; helical-scan color recorders are available, but the methods of signal handling are less satisfactory for this application.

Although not germane to the principal subject of this paper, it is worth mentioning that the audio track of the recorder also is available for recording data and is indeed used in our application. A commercial equipment accepts slowly varying analog signals from a concurrent experiment and frequency modulates an audio carrier for each input. These audio signals are recorded on the audio track and reconstructed later as analog signals, which may themselves be digitized. The data thus recorded are absolutely fixed in time relative to

[5] *Yoshio Sawaji, EIAJ Standards for 1/2 Inch Videotape Recorders, J. Soc. Motion Pict. Telev. Eng.,* **79** *(December 1970), 1091-1093.*

the video signal; this is a commanding advantage over the use of a separate recorder, no matter what timekeeping scheme is used.

1.3 Video Processor

The Video Processor performs distinctly different functions during recording and playback. While recording, it inserts a nonreturn-to-zero (NRZ) binary code corresponding to the frame number and provides triggers to the injection laser modulator and R7912 sweep in synchrony with the advent of a frame. During playback, it recovers the frame number, restores the integrity of the black-to-white transitions of the video signal, translates these transitions to transistor-transistor-logic (TTL) levels, and recovers the timing information necessary to the proper operation of the Digitizer/Interface circuitry.

1.4 Video Digitizer and Computer Interface Unit

During the playback procedure, the Digitizer/Interface divides active scan time of each line into 256 equally long intervals (pixels) and seizes the four 8-bit bytes corresponding to the four edges produced as the reading beam crosses the two traces. In addition, at the outset of each frame, it seizes the 16-bit frame number, divides it into two 8-bit bytes, and inserts them into the output data stream at an appropriate place. (The frame number is repeated to provide a check.) A first-in, first-out buffer memory (FIFO) 8 bits wide is provided to take advantage of a block sequential reading capability of the Interdata 7/32 computer.

2. DESCRIPTION OF VIDEO PROCESSOR

2.1 Nature of Signals

The Video Processor operates during both recording and playback, in the first instance to number frames and provide triggers to the experiment, in the second to recover timing data and frame numbers and to restore the levels of the black-to-white transitions generated by the trace crossings. Many of the circuits necessary to achieve these functions are common both to recording and to playback and were therefore more economically implemented in one package. For clarity, the recording functions are described first. In order that the operation of these circuits may be fully understood, it is necessary to consider the nature of National Television Standards Committee (NTSC) television signals and the waveforms encountered in the transmission of these signals.

As in motion picture parlance, each complete television picture is called a frame. Each frame contains 525 lines and requires 1/30 s to be completely scanned. To reduce the apparent flicker of the image at the viewer's eye, the frame is presented in two fields such that if the lines of the image were numbered sequentially top to bottom, the odd-numbered lines would fall in the first field and the even-numbered lines would fall in the second field. A picture scanned in this way is said to be interlaced 2:1. Thus, the field repetition rate, f_v, is twice the frame rate, f_f, or in this case 60 Hz. Interlacing is achieved by making the line rate, f_h, equal to an odd half-multiple of the field repetition rate. Here,

$$f_h = (525/2)f_v$$

or, for $f_v = 60$ Hz,

$$f_h = 15{,}750 \text{ Hz}.$$

A partial drawing of a standard television signal is given in figures 4 and 5. That part of the waveform above the blanking level is considered to be video (that is, gray-scale picture information), while that which falls below the blanking level contains the synchronizing information. A typical line containing video information is shown in figure 5. The line is said to begin at the leading edge of the horizontal synchronizing pulse, h sync, which is about

4.76 μs wide. The horizontal blanking pulse overlaps the h sync pulse in order to permit resetting the horizontal sweep generator. Thus, the active line begins some 9.52 μs after the leading edge of the h sync pulse and ends about 1.59 μs before the leading edge of the next h sync pulse. Similarly, at the beginning of a field, some 21 lines are blanked (vertical blanking interval) to permit retracing of the vertical sweep, although the field vertical synchronizing information itself occupies only 3 lines.

Several features of the synchronizing waveform are of interest. Note the six narrow pulses ("equalizing pulses") that occur during the three lines preceding and following the field synchronizing interval and the positive-going pulses ("serrations") that interrupt that interval. These pulses were originally included in the composite waveform because the technology of the year 1945 forced industry to adopt certain expedients in order to achieve proper synchrony of television receivers with the transmitted signal. At this writing, neither

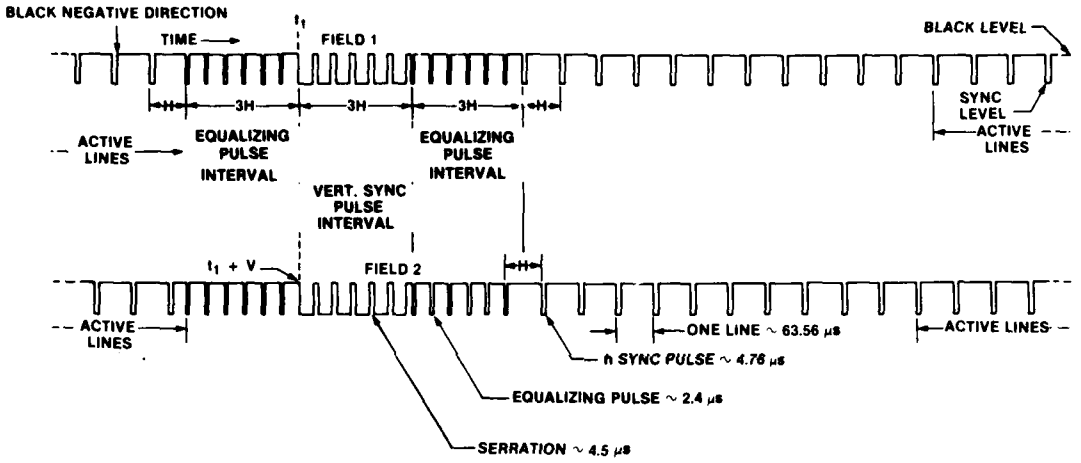


Figure 4. Standard television signal—vertical synchronizing interval.

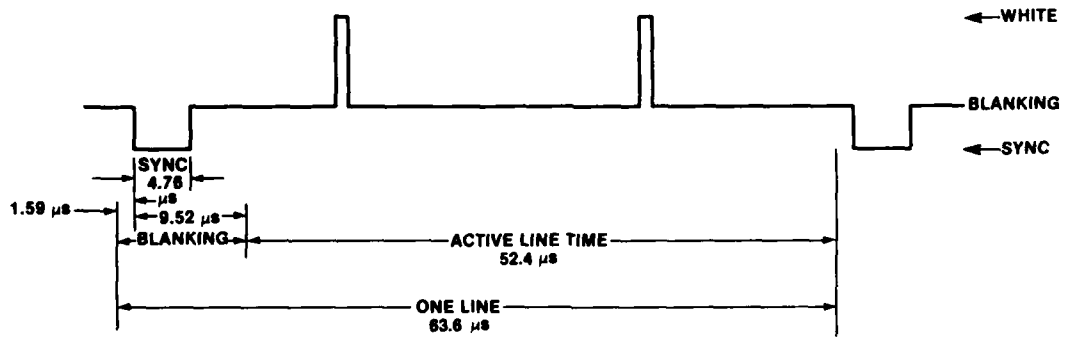


Figure 5. Typical line of television signal containing two trace crossings.

serrations nor equalizing pulses are strictly necessary to the correct operation of a television set, provided that the design takes account of the omission; however, these signals are included in a standard waveform and are in this instance useful to us, as will become evident.

Remark, for example, a difference between the vertical blanking and synchronizing waveforms associated with fields 1 and 2 (fig. 4). The leading edge of the serrated field sync pulse is aligned with an h sync edge in field 1; in field 2, it falls in the center of a line. Differences of this character are a result of the interlacing process and may be used retrospectively to discover whether the field is even or odd. We refer to this in the detailed discussion of circuit operation, but it is sufficient here to remark that our design requires that only two pieces of information be recovered from the synchronizing waveform: the beginning of each frame must be known, and the beginning of each line within the frame must be known. As is discussed in section 2.2, it is advantageous to distinguish field 1 at the first h sync pulse after the field sync pulse. This pulse is given the name "frame-start pulse."

2.2 Synchronization Processing

For the following discussion, the reader is asked to refer to figure 6, a block diagram of the Video Processor operating in the acquisition mode, and to figure 7, the complete schematic.

While recording, all timing information is derived from the composite sync output of the R7912. This, however, is a standard EIA waveform, 4 V peak to peak (pp) across 75 ohms, and is alternating current (ac) coupled so that it cannot drive the synchronizing logic directly. Passing the EIA sync through the same sync separator used for playback sync extraction has the effect of shifting its level to

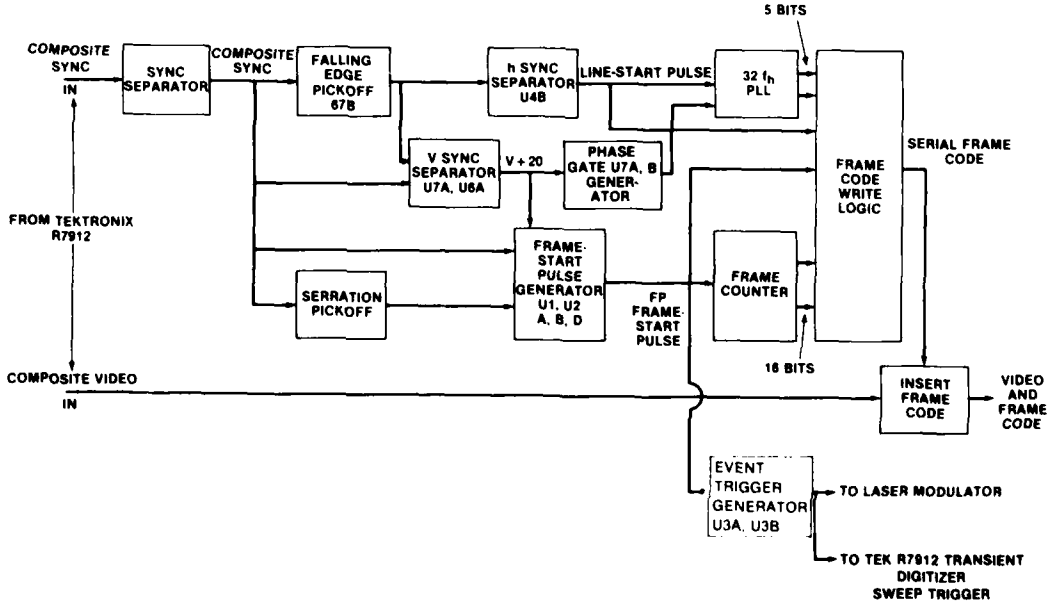


Figure 6. Video Processor acquisition mode, block diagram.

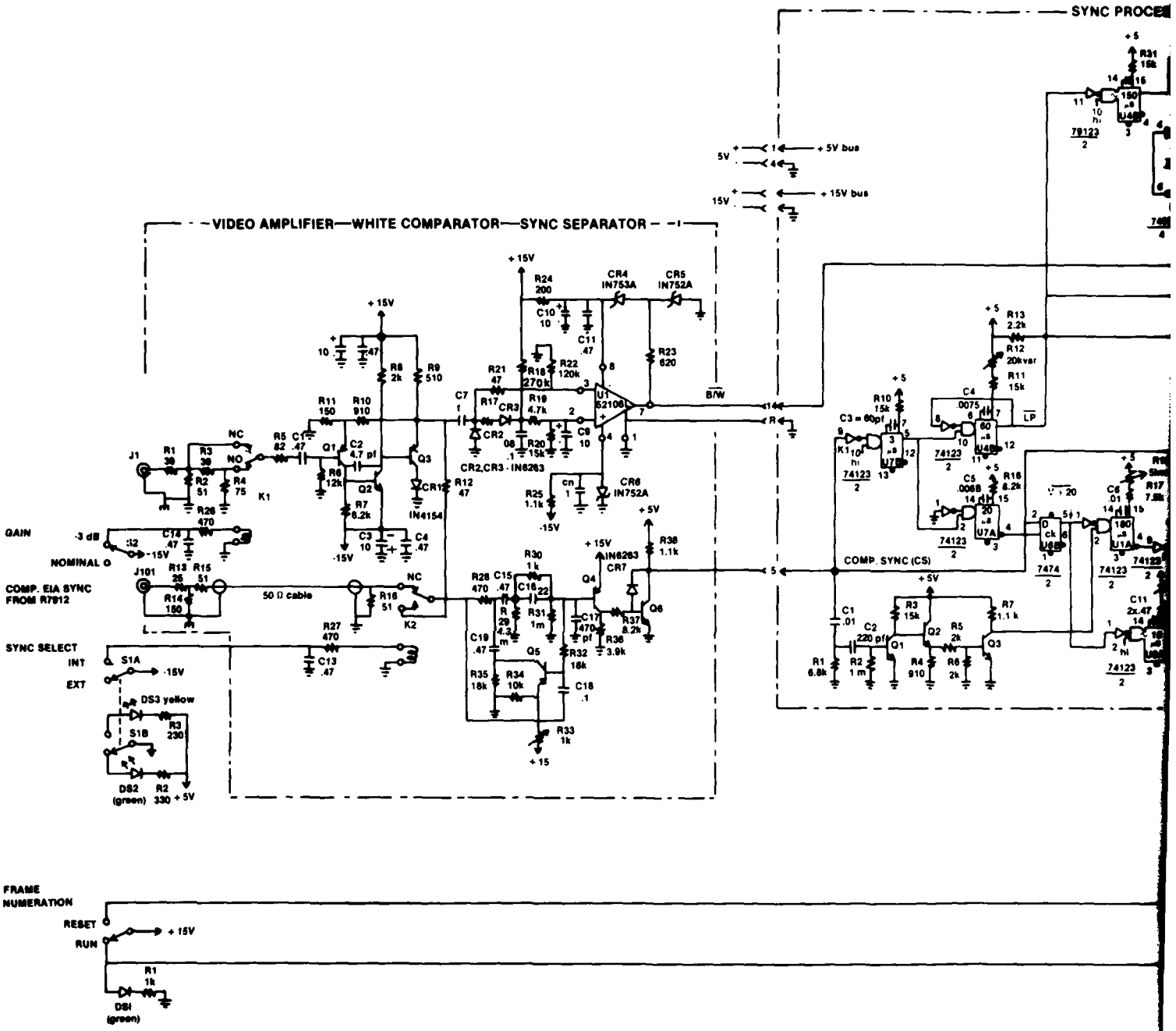


Figure 7 Video Process

NOTES:

ALL PNP TRANSISTORS ARE 2N3906. EXCEPT FOR THE TRIGGER EMITTER FOLLOWER, A 2N3663, ALL NPN TRANSISTORS ARE 2N3904.

PANEL MOUNTED COMPONENTS ARE NUMBERED FROM 1 ON THE FRONT PANEL AND FROM 101 AT THE REAR SO THAT J1 IS ON THE FRONT AND J102 IS AT THE REAR.

⏚ REPRESENTS CASE GROUND.

⏚ REPRESENTS LOCAL GROUND, AS ON A PRINTED CIRCUIT BOARD ASSEMBLY.

TO ENHANCE READABILITY OF THE DRAWING, THE FOLLOWING ARE NOT SHOWN:
- MOST POWER SUPPLY BYPASSES
- THE DC SUPPLIES THEMSELVES
- PULLUPS ON UNUSED TTL INPUTS AND CLEARS
- REDUNDANT GROUNDS
- POWER AND GROUND CONNECTIONS TO THE LOGIC INTEGRATED CIRCUITS

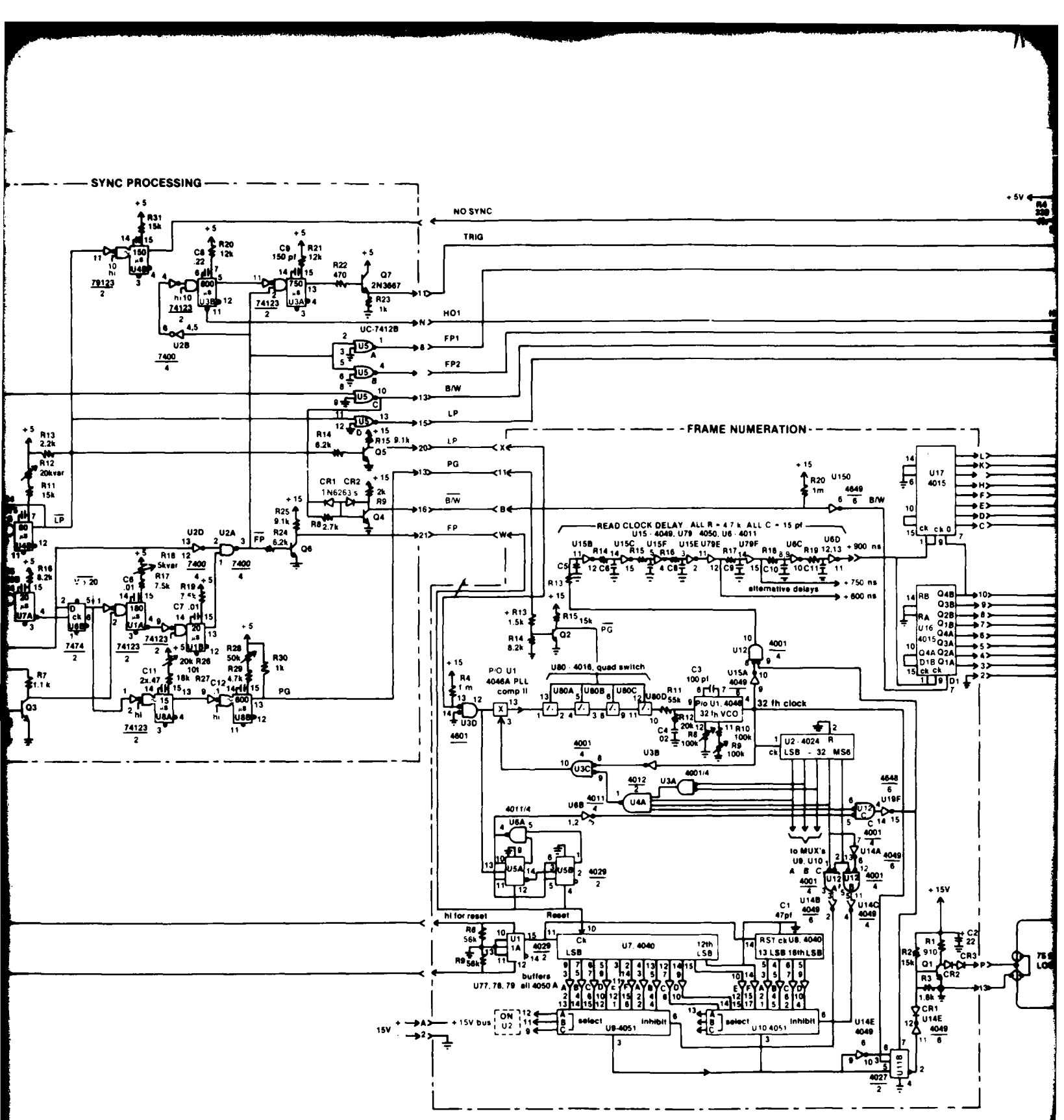
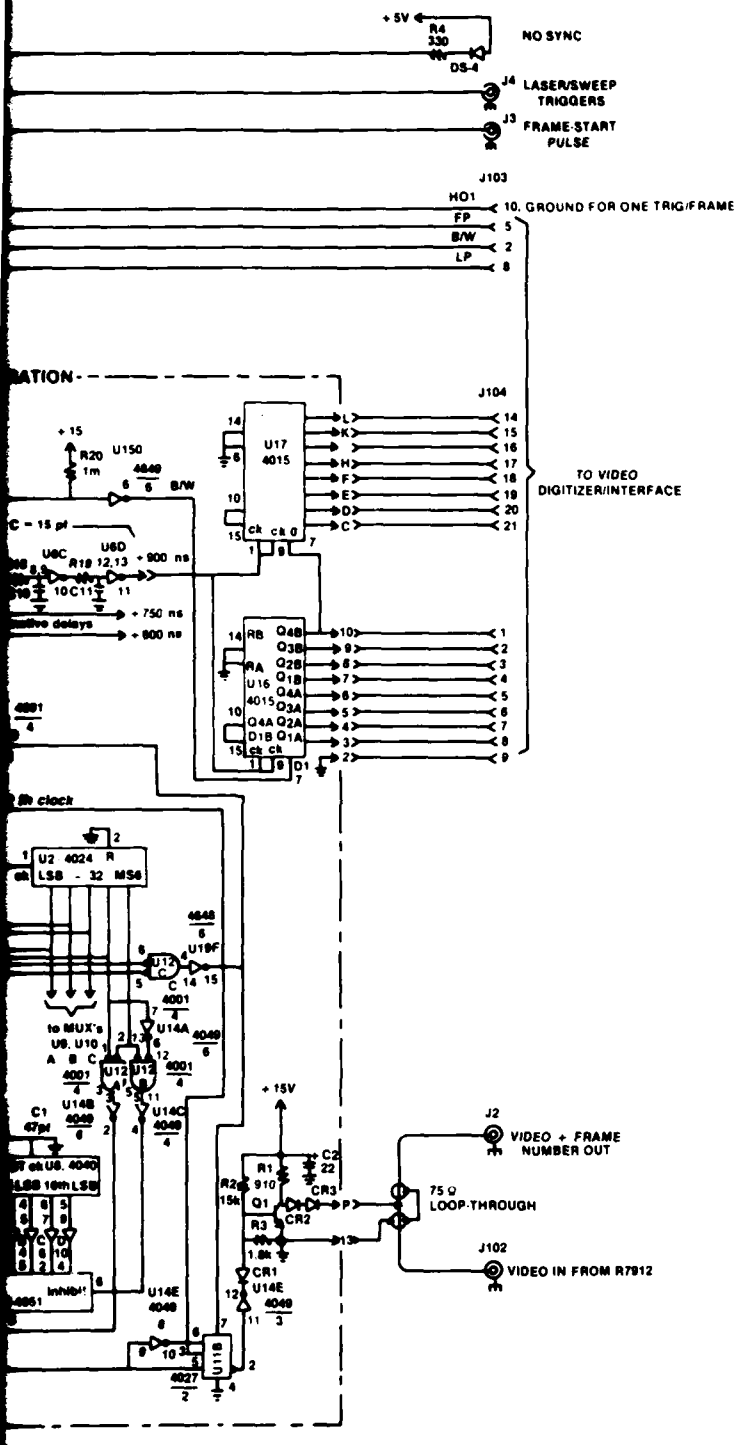


Figure 7 Video Processor, schematic diagram

11/12 2


+ 5V
R4
330
DS-4
NO SYNC
J4
LASER/SWEEP
TRIGGERS
J3
FRAME-START
PULSE
J103
HO1
FP
B/W
LP
10. GROUND FOR ONE TRIG/FRAME
5
2
8
ATION
J104
TO VIDEO
DIGITIZER/INTERFACE
+ 15
R20
1m
U15D
4049
B/W
C = 15 pf
U6C
U6D
R19 12,13
+ 900 ns
10C11
11
+ 750 ns
+ 900 ns
U17
4015
U16
4015
4001
4
clk
LSB - 32 - MSB
U2 4024 R
to MUX's
U9, U10
A B C
U19F
U14A
U14B
U14C
U14E
C1
47pf
R1
910
R2
15k
Q1
CR3
CR2
R3
1.8k
CR1
C2
22
+ 15V
J2
VIDEO + FRAME
NUMBER OUT
75 Ω
LOOP-THROUGH
J102
VIDEO IN FROM R7912
4027
2

the standard TTL level. Additionally, the relative delays incurred during recording and playback tend to be equalized. This signal is operated on by the sync processing circuits to extract line-start pulses (LP's) and frame-start pulses (FP's). The means by which this extraction is done is of some interest.

To extract LP's, the composite synchronizing signal first triggers U7B, a one-shot, to produce a 3-μs pulse for each falling (that is, true) sync edge. The h sync separator is merely a nonretriggerable one-shot (U4B) having a period greater than half a line. Thus, edges generated by those equalizing pulses and serrations that fall in the middle of a line do not trigger the one-shot, nor do noise pulses falling within the time-out. (The edge pickoff is made necessary by the characteristics of the nonretriggerable connection.) The output of U4B, buffered to both complementary metal-oxide semiconductor (CMOS) and TTL levels, is the LP.

Derivation of the FP is somewhat more complex (fig. 8). In principle, the serrations are separated from the composite synchronizing waveform, the last serration then initiating the generation of a delayed 20-μs gate (U1A, U1B) overlapping the 10th line sync pulse of field 1, that is, the first full-width h sync pulse of that field (fig. 8d,e). (U1A is actually retriggered by all serrations, but the time-out begins from the last serration.) ANDing the 20-μs gate with the synchronizing waveform (U2A, U2D) produces this one pulse as output if and only if the field is odd (fig. 8f). This system worked without difficulty when the applied synchronizing waveform was free of spurious signals, as during the recording process. However, it became evident that, during playback, the spurious transients in the VTR output would produce adventitious outputs from the serration detector and, hence, many opportunities for the generation of a false FP. This is in the utmost degree undesirable since it causes loss of that frame in the

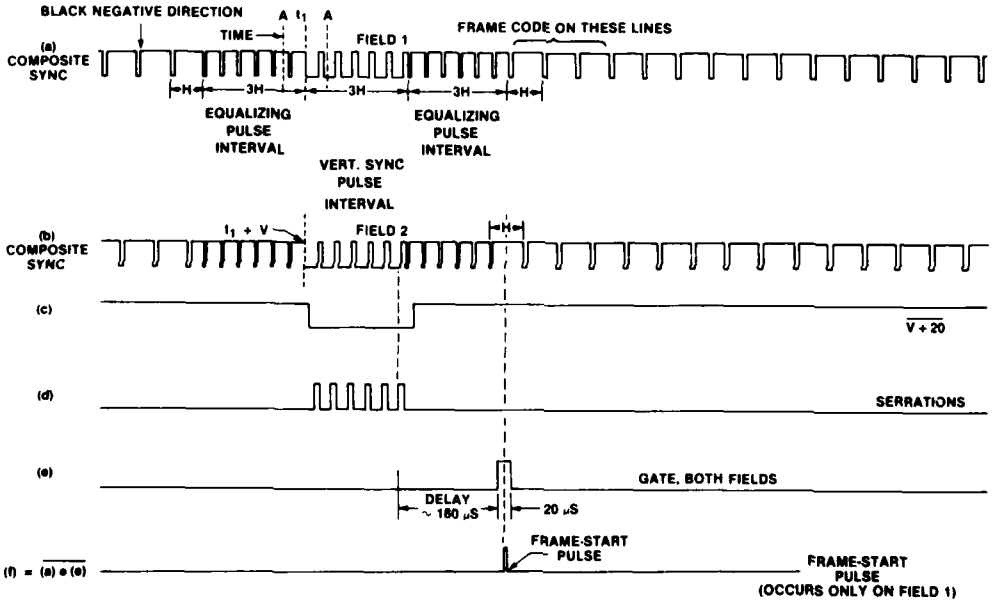


Figure 8. Derivation of frame-start pulse.

Digitizer/Interface. Accordingly, a signal related to the field (that is, vertical) synchronizing interval was used to arm the delay gate generator for a brief part of each field. This arming signal is generated by U7A and U6A, which comprise a field sync separator, the Q output of U6A going low 20 μs after the field vertical sync interval begins and rising 20 μs after the end of the interval (fig. 8c)—hence, the name V + 20. It was determined experimentally that this improves matters by a factor of about 140 so that on the average only one frame is lost in every 4500 frames. This amounts to the loss of 12 frames over a 0.5-hr tape, which is considered acceptable.

Triggers for the laser modulator and R7912 time base are generated by one-shots U3A and U3B. The operation of this circuit is evident from the detailed schematic diagram (fig. 7). U3A generates two triggers per frame, the first occurring at the falling edge of $\overline{FP}$ (that is, the leading edge of FP) and the second occurring about 800 μs later, when U3B times out. A useful feature of this circuit is that holding U3B clear (that is, grounding the H01 line) deletes the second trigger. This was later found helpful for remote selection of one trigger per frame.

A pair of one-shots (U8A, U8B) generates a phase gate pulse (PG) about 600 μs wide delayed nearly from one vertical synchronizing interval to the next. Although this circuit functions at all times, its inclusion has to do with the recovery of frame numbers during playback and is therefore described in section 2.6.

Lastly, one-shot U4B is continually triggered by LP. Because its time-out is greater than one line, its output remains high unless television sync is absent. In that case, its output goes low, lighting red light-emitting diode (LED) DS4, the NO SYNC indicator. This warning was included so that an operator setting up the equipment in the field should see nothing lit on the front panel but green LED's. Thus, the indicators for POWER, EXTERNAL SYNC, and FRAME NUMERATION ON are all green LED's

2.3 Frame Numeration

The synchronizing logic was implemented with TTL devices to avoid the large propagation delays of the metal-oxide semiconductors (MOS). The frame numbering circuit, on the other hand, was constructed in the CMOS to save power. This was feasible because the various propagation delays are of no consequence to the design. Proper operation of the phase-locked loop (PLL) required a supply of +15 V so that level shifters were required to supply LP, FP, PG, and (during playback) detected white levels at the proper levels (LP', FP', PG', and B-W') to operate the CMOS logic. (Priming indicates CMOS levels.)

The operation of the frame numbering circuit is readily described (fig. 7). First, LP' is introduced via U3D to the PLL comprising U1, U2, U3, U4, U80, and Q2. (The function of the last two parts is discussed in section 2.6; for this discussion, assume that U80, a quad transmission gate, always conducts.) The PLL runs at 32 f_h, or about 504 kHz. Counter U2 divides this frequency by 32; gates U3A, U3B, U4A, and U3C decode binary state 11001, which serves as the edge that the PLL locks to LP'. The purpose of this offset is to establish that states 00000 through 01111 (decimal 0 through 15) will fall in the middle of the active line time. This offset much simplifies the output circuitry.

Turning now to the frame counting circuit, FP' is led to U7, a 12-bit counter. U7 and U8 together comprise a 16-bit ripple-through counter, which advances 1 bit at each frame. Each occurrence of FP' also resets flip-flops U5A and U5B, which are connected to count three LP's and lock on the fourth. The result is that the output of U6A is high for the three lines following FP', these three lines being those upon which the frame code is to be written. This signal is combined with the most

significant bit (MSB) of counter U2 in gates U6B, U12C, and U14F to provide a signal that is low only during that portion of a line during which data are to be inserted. This write enable signal inhibits the output flip-flop U11B at all other times.

Returning now to frame counter U7-U8, the 16 output lines are connected to the two CD4051 8:1 multiplexers, U9 and U10. Since these multiplexers are tristate, it is feasible to connect their outputs together and enable only one at a time. Thus, the bit-select lines of the multiplexers are driven from the three least significant bits (LSB's) of U2, while their inhibit inputs are driven in such a manner that first U9 is enabled, and the first 8 bits of the frame code are read out; then U10 is enabled, and the last 8 bits of the frame code are read out. In this way, a serial stream of 16 bits is read out of the multiplexers on each line of the television frame. This stream is applied to output flip-flop U11B, which is inhibited from changing state, except for that interval in the midst of the three lines following an FP during which the data stream is actually present. U2, controlling the multiplexers, changes state on the falling edge of the 32 f_h clock, while U11B changes state on the rising edge, thus avoiding a potential race condition. The output of U11B is taken through inverting buffer U14E, which has sufficient sink capability to interface with the bipolar output stage comprising Q1 and associated parts. Normally, Q1 is on and its collector is low so that CR2 and CR3 do not conduct. When Q1 is driven off by the white (low) signals at its base, current from the +15 V supply can flow via R1, CR2, and CR3 into the video circuit. The current chosen is sufficient to produce a white-level signal in a 75-ohm load. The video outputs of the R7912 are not reverse terminated so that this current is developed across 75 ohms, not one-half of 75 ohms, as it would be if both the source and the load were matched to the line. The line length from the R7912 to the point where the frame code is inserted is kept short to avoid troublesome reflections.

2.4 *Video Processor--Digitizing Mode*

Let us now consider what additional functions the Video Processor must perform while digitizing. Digitizing is not limited to taped signals already acquired; it is perfectly feasible to connect the video signal from the R7912 via the frame numeration circuit directly to the same video input that is used when digitizing from the VTR. Indeed, much development work was accomplished in exactly this way. The Digitizer/Interface requires that four signals be derived from the composite video signal: (1) FP's, (2) LP's, (3) detected white levels corresponding to the trace crossings, and (4) frame numbers in 16-bit parallel form. It is convenient to describe, first, the video input circuits and, second, the additions necessary for the recovery of frame numbers.

2.5 *Video Input Circuits*

The input video board accepts video plus frame code either from the VTR (0.9 Vpp) or from the R7912 (1.36 Vpp), external EIA composite sync, and two control signals—one for video gain selection to compensate the disparity between the two video signal amplitudes and the other for selecting whether sync will be derived from input video or from EXTERNAL SYNC (that is, the R7912). Outputs are (1) detected white levels and (2) either composite sync or composite video. The first signal is buffered and used by the digitizer circuitry and by the frame code recovery circuit; the second signal is fed to the sync separator and thence to the sync processing board so that the timing information used to control both digitization and the frame coding and decoding may be recovered.

Because of the disparity in amplitude between the VTR video and the video from the R7912, a switched input attenuator was provided to change the signal level applied to the input video amplifier. This amplifier, comprising Q1, Q2, Q3, and associated parts, has a

nominal gain of about 7.1. Taken in conjunction with the switched attenuator, the overall voltage gain is either 3.4 or 2.2, depending on the state of gain select relay K1. This change yields a nominal video level of 3 Vpp at the input of the white comparator circuit. The signal is ac coupled to the comparator circuit by C7 and direct current (dc) restored on the sync tip by CR2, a low-drop Schottky diode. The dc-restored video is applied essentially unchanged to the input of comparator U1; also, peak white signals cause CR3 to conduct, changing C8 to peak white (less the diode drops). A fraction of this signal is applied to the noninverting input of the comparator. (Resistor R18 prevents C8 and C9 from discharging completely during the vertical blanking interval.) Thus, the output of the comparator drops whenever the video signal exceeds about 50 percent of the peak white level.

The video amplifier also drives the synchronizing pulse separator when INTERNAL SYNC is selected. The sync pulse separator is a conventional peak-detecting type incorporating a rudimentary noise inverter. This method of sync separation is subject to timing errors in the presence of random noise on the sync tips. Jitter of 50 ns or so relative to the 50 percent point of the leading edge of the sync pulse is common when the input signal is from a VTR of the type used here. When truly precise timing is sought, other means of sync recovery are used. Separated composite sync at TTL levels is carried to the sync processing board, where the timing signals FP and LP are derived in precisely the same manner as described previously. These along with the output of the white comparator are buffered and cabled out to the Digitizer/Interface.

A remarkable and highly interesting example of video signal processing technology is the time base corrector (TBC) used by television stations to bring the video from helical-scan recorders up to broadcast standard, at least as regards timing. To give an example of the performance attained, the cumulative timing error in the VTR output may amount to a jitter of 30 μs at the end of a frame, that is, the last sync pulse of a frame may be half a line from where it should be, even though the error within each line of the frame is small. A TBC reduces this error by more than 10^4. This processing, in general, involves 8- or 9-bit digitization of the analog video input every 90 ns or so, the rate varying in step with the input sync, reading the digitized pixels into a digital store about 2×10^3 bytes long, reading out the store, and converting back to analog at a rate locked to the station master sync signal. It is customary to strip the degraded original sync and substitute noise-free station sync in its place. What is interesting about this is that the universally preferred method of sync separation from the corrupted video is by means of a comparator, the threshold of which is set about halfway between the blanking level and the sync tip. No noise protection whatever is used, and the separated synchronizing signal contains many noise pulses. All noise rejection is provided by subsequent signal processing. This design philosophy, though resulting in circuits of astonishing redundancy and complexity, unquestionably provides the most precise timing information which it is possible to derive from a video signal.

2.6 *Frame Number Recovery*

In principle, recovery of the frame numbers from video tapes is quite simple to implement and requires few additions to the frame code circuit board. The basic circuit required for this comprises U15, U12D, part of U6, part of U79, U16, and U17. The last two circuits make up a 16-bit serial-in parallel-out shift register. White levels detected by the white comparator circuit previously described are shifted into this register by a burst of clock pulses. Note that the clock burst is generated by gating the write enable signal of the frame numeration circuit with the 32 f_h clock and delaying the result so that the clock transitions fall in the proper relation to the edge of the bit

cells of the serial frame code. The parallel outputs of the shift register are stable at the end of each burst of clock pulses; indeed, the last copy of the frame code is held throughout the frame because no further clocks are generated until the first copy of the next frame number arrives.

In practice, this system was found to be susceptible to noise pulses present on the VTR output, and a retrospective modification was necessary. This problem arises from the nature of helical-scan VTR's. To describe the operation of these machines is not within the scope of this paper. It suffices to state that (1) two recording-playback heads are used, (2) the heads and the tape move so that each head contacts the tape about half the time, (3) it is necessary during playback to switch off the head not momentarily in contact with the tape, and (4) the head-switching process generates two spurious transients at the end of each field. These spurious signals are typically from less than 1 to several microseconds in length and may be several times the signal amplitude. On a video signal extending from 0 V (sync level) to +1 V (peak white), it is not unusual to see head-switching transients extending down to −1 V or up to +2 V. The location of these signals in the frame is somewhat variable, depending upon the recorder design and alignment. A significant difference may be observed when a tape made upon one machine is played upon a nominally identical machine. However, the recorders used in this project typically switch within the last 10 active lines of each field.

These pulses are not entirely suppressed by the noise inverter of the sync separator circuit, nor does the h sync separator ignore those pulses that fall after its time-out. Noise pulses falling near a sync edge are considered to be a sync edge and drive the PLL of the frame numeration circuit far from lock. (Reducing the PLL gain or increasing its time constant is no solution, because true variations in sync edges cannot then be followed.) With the PLL far from lock, the chance of correct frame number recovery is nil. As becomes evident in section 3, correct recovery of frame number is essential to the proper operation of the Digitizer/Interface circuitry.

An ad hoc solution was applied: the correcting mechanism of the PLL was disabled during the 10 or so lines during which such transients might occur.* A disabling gate is generated by one-shots U8A and U8B on the sync processing board by delaying from the V + 20 signal. This delayed pulse, PG, drives a quad transmission gate (U80) in series with the phase detector output so that no correcting pulses are applied to the voltage controlled oscillator (VCO) during this interval. In effect, the loop coasts at its previous lock frequency. Correction is reestablished near the beginning of the field synchronizing interval. Thus, about six lines are available to restore lock before the frame code reappears. This arrangement has been observed to make possible the recovery of frame numbers even from tapes of very poor quality.

A further consequence of the head-switching process is that if a tape is played with incorrect tension, a kind of mistracking will result. This is known in the video industry as "skew" because of its effect of skewing the top of the television picture to the left or right. This is described by Sadashige[6] and Cook,[7] but should be considered briefly here. Suppose that the first head of the VTR has just finished reading a field and that the second head is commencing to read the field laid down in the next track.

[6]Koichi Sadashige, *The Effect of the Choice of Tape Format on Broadcast Video Recording*, IEEE Broadcasting, **BC-20** (March 1974), 12-16.

[7]Thorsten P. Cook, *An Automatic Skew Corrector for Helical Scan Cassette Video Tape Players*, J. Soc. Motion Pict. Telev. Eng., **82** (April 1973), 287-289.

*A more positive remedy would have been to number the frames not with an NRZ binary code, but with some form of self-clocking code so that the clocking information would be inherent in the bit stream representing the frame number. Various constraints, but primarily the overriding necessity to reduce data already labelled with an NRZ code, prevented our adopting this simple solution.

If the tape tension is incorrect, the tape will stretch minutely so that the second head does not start at the right point relative to the information on the tape. The effect of this is to produce a step change in the phase of the horizontal sync pulses and hence to unlock the PLL. Nor is the mistracking necessarily caused by misadjusted equipment: often it is the consequence of changes in tape mechanical properties incurred when tapes made under field conditions are brought into the laboratory, where temperature and relative humidity are closely controlled.

Three remedies for this condition are possible. First, the VTR tape tension may be adjusted mechanically as required for any portion of a tape. An automatic means of adjustment is described by Cook.[7] Alternatively, if the recorder can be modified, the range of the tracking control might be extended. That is, the capstan servo loop might be altered to increase its operating range and authority. Second, a posteriori correction of the signal by electronic means is feasible: some of the most modern time base correctors are designed to recognize and correct step phase error. This is the simplest method of dealing with the problem, but it is also unquestionably the most expensive. Third, it is possible to redesign the frame numbering scheme so that it will be immune to step phase errors in the line sync rate. This is conceptually the most attractive remedy since its successful realization would greatly enhance the operational use of the recorders. For example, the easy interchange of tapes and recorders would obviously benefit system reliability.

3. VIDEO DIGITIZER AND COMPUTER INTERFACE UNIT

The easiest way to explain the operation of the video digitizer is to examine the collection of data during a typical line of frame; frame numbers are read similarly. After the operation during single lines is understood, insight into the operation during an entire frame may be gleaned. The overview is completed by discussions of the various error conditions, of the way that processing is started, and of a method of slowing the data rate for compatibility with a floating-head disc. Throughout this exposition, reference is made to figure 9, a block diagram of the interface, and figure 10, a complete schematic. All labels of signals and components discussed here may be found in figure 10.

The essential idea underlying the retrieval of the data contained in each line is to divide the active line time into 256 cells and to note in which cells each of the two black-to-white transitions occurs and in which each of the two white-to-black transitions occurs. Since $256 = 2^8$, each cell has an 8-bit number associated with it. The cell numbers of the four transitions are the four data bytes required for each line. The active line time is divided into 256 discrete intervals by use of the data counter (D4 and D5 in fig. 10); the duration of the active line time is 52.433 μs. Each cell is therefore 204.82 ns long, which implies a clock frequency of 4.8824 MHz. This clock is implemented as a two-phase, nonoverlapping clock having phases ϕ_1 and ϕ_2. The timing of the interface is arranged so that at the beginning of each active line time (of a line having data), the data counter contains the binary number 00000000, and the multiplexer channels the output of the data counter to the four data registers. Transitions of the video signal (black to white and white to black) cause strobing of the four data registers. A strobe pulse to the data register causes the register to hold the value of the data counter at the time of the strobe pulse.

There is a critical race between the black-to-white signal and the state of the data counter (D4 and D5). The transitions of the black-to-white signal are synchronized with the ϕ_1 clock by flip-flop D27. The data counter is

[7] Thorsten P. Cook, An Automatic Skew Corrector for Helical-Scan Cassette Video Tape Players, J. Soc. Motion Pict. Telev. Eng., **82** (April 1973), 287-289.

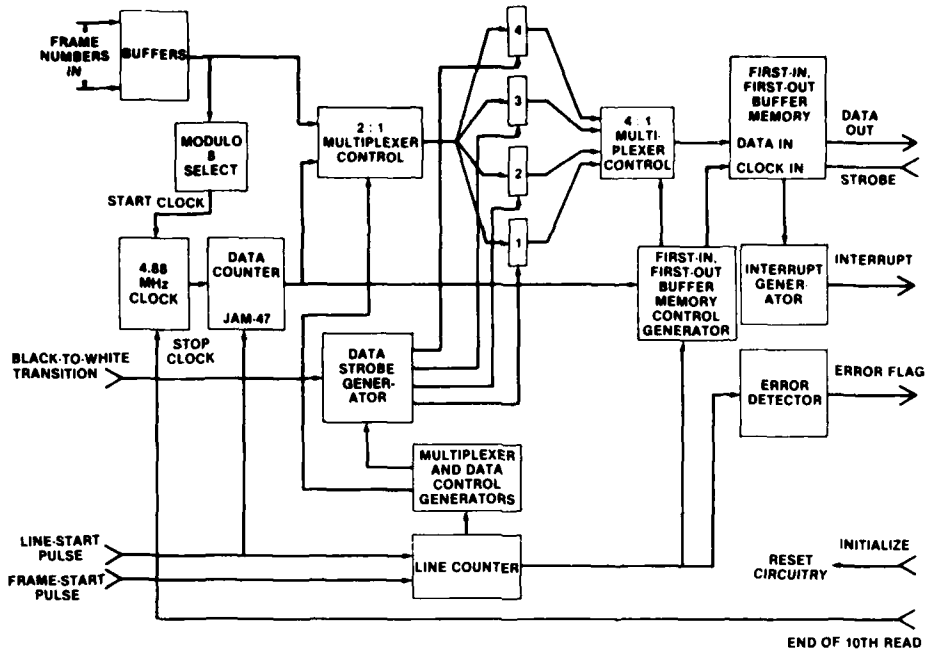


Figure 9. Block diagram of Video Digitizer and Computer Interface Unit.

actuated by ϕ_1 also. As an example of the hardware used to implement the strobing of the data registers, we call attention to D25, D30, and D32. For clarity and ease of discussion, propagation delays are ignored. At the beginning of each line, D25 and D30 are both in the 0 state. The occurrence of the first ϕ_1 clock pulse after the black-to-white transition goes to the 1 state causes D25 (1, 2, 3, 14, 12) to toggle, leaving D25 in the 1 state. The output of D25, being in the 1 state, enables gate D30 (8, 9, 10) and at the next ϕ_2 clock pulse appears at the output of D30, whence it is routed through D45 (4, 5, 6) to the strobe input of the first data register; the same ϕ_2 clock also sets D32 to the 1 state, which enables D30 (11, 12, 13). After the events just described, the ϕ_1 clock is reproduced at the preset input to D25. Since the preset input dominates the clock input and since the clock input to D25 is actuated only coincidently with ϕ_1, D25 is held in the 0 state for the remainder of the line. The effects of the entire sequence of events are that (1) at most one strobe pulse per line is issued to data register one and (2) this strobe pulse can occur only during ϕ_2. The strobe pulses to the other data registers are generated in like manner with allowances being made for differences in polarity and number of transitions of black to white.

Thus, at the end of a line having data, if all goes well, the cell number of the first black-to-white transition is in data register 1, the cell number of the first white-to-black transition is in data register 2, the cell number of the second black-to-white transition is in data register 3, and the cell number of the second white-to-black transition is in data register 4. These are D10, D11, D12, and D13 in figure 10. At this point, the task is to put the contents of the four data registers into the FIFO during the horizontal blanking interval.

The transfer of the contents of the four data registers to the FIFO occurs during the 9.53 μs between the beginning of the next line at LP and the begininning of the next active line time. Since 52.433 μs corresponds to 256 time cells, 9.53 μs corresponds to 46.53 time cells; the closest integer to 46.53 is 47. Therefore, if the data counter is preset at −47, 11010001 in binary, then the counter contains 00000000 when the active line time begins. Since the FIFO can accept one 8-bit byte every 500 ns, forty-seven 200-ns time increments are more than sufficient to accomplish the transfer.

Each time cell is 204.82 ns long; two cells last approximately 400 ns, and four cells last approximately 800 ns, long enough for the FIFO to accept one byte. Hence, the (positive) transitions of the third LSB of the data counter are used as the clock for the FIFO. Furthermore, since the fourth and fifth LSB's change coincidently with the negative transitions of the third LSB, they are used to control the 4:1 multiplexer (without, incidently, any further decoding since all that is required is routing the signals from the four data registers in accordance with the 2-bit number corresponding to the fourth and fifth LSB's during the appropriate positive transition of the third LSB). Table 1 shows the details of this relationship.

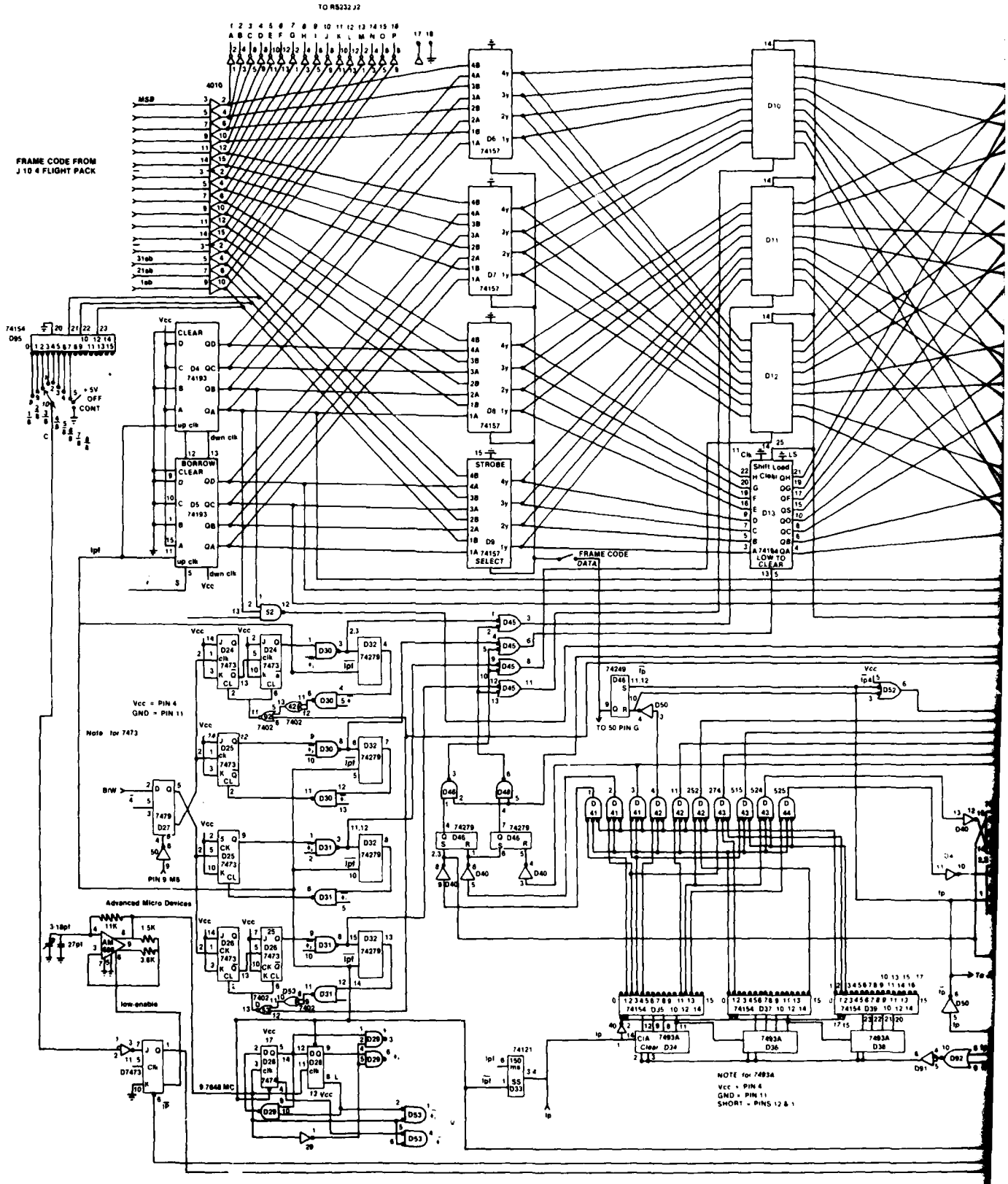
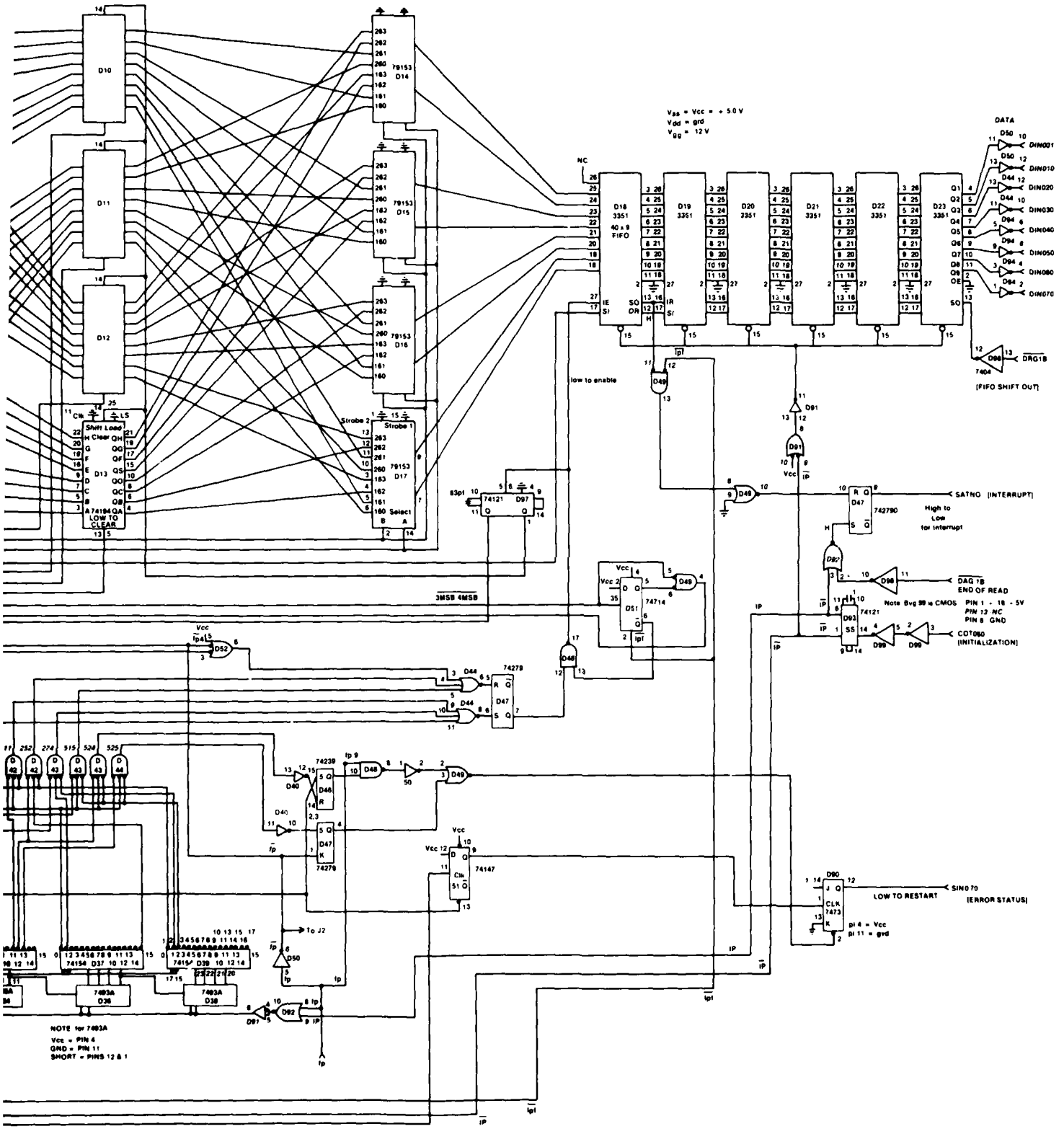


Figure 10 Complete schematic diagram of Video Digitizer and Computer Inter



Schematic diagram of Video Digitizer and Computer Interface Unit

21/22 1 2

TABLE 1. RELATIONSHIP OF DATA COUNTER STATES TO FIRST-IN, FIRST-OUT BUFFER MEMORY AND MULTIPLEXER TIMING

MSB			Multiplexer		Clock for FIFO		LSB	Comment
1	1	0	1	0	0	0	1 = −47	Leading edge of LP presets −47 and enables FIFO
1	1	0	1	0	0	1	0	
1	1	0	1	0	0	1	1	
1	1	0	1	0	1	0	0	Shift register 1
1	1	0	1	0	1	0	1	
1	1	0	1	0	1	1	0	
1	1	0	1	0	1	1	1	
1	1	0	1	1	0	0	0	
1	1	0	1	1	0	0	1	
1	1	0	1	1	0	1	0	
1	1	0	1	1	0	1	1	
1	1	0	1	1	1	0	0	Shift register 2
1	1	0	1	1	1	0	1	
1	1	0	1	1	1	1	0	
1	1	0	1	1	1	1	1	
1	1	1	0	0	0	0	0	
1	1	1	0	0	0	0	1	
1	1	1	0	0	0	1	0	

TABLE 1. RELATIONSHIP OF DATA COUNTER STATES TO FIRST-IN, FIRST-OUT BUFFER MEMORY AND MULTIPLEXER TIMING (CONT'D)

MSB			Mulitplexer		Clock for FIFO		LSB	Comment
1	1	1	0	0	0	1	1	
1	1	1	0	0	1	0	0	Shift register 3
1	1	1	0	0	1	0	1	
1	1	1	0	0	1	1	0	
1	1	1	0	0	1	1	1	
1	1	1	0	1	0	0	0	
1	1	1	0	1	0	0	1	
1	1	1	0	1	0	1	0	
1	1	1	0	1	0	1	1	
1	1	1	0	1	1	0	0	Shift register 4
1	1	1	0	1	1	0	1	
1	1	1	0	1	1	1	0	
1	1	1	0	1	1	1	1	
1	1	1	1	0	0	0	0	Disable FIFO
1	1	1	1	0	0	0	1	
1	1	1	1	0	0	1	0	
1	1	1	1	0	0	1	1	

TABLE 1. RELATIONSHIP OF DATA COUNTER STATES TO FIRST-IN, FIRST-OUT BUFFER MEMORY AND MULTIPLEXER TIMING (CONT'D)

MSB			Multiplexer		Clock for FIFO		LSB	Comment
1	1	1	1	0	1	0	0	
1	1	1	1	0	1	0	1	
1	1	1	1	0	1	1	0	
1	1	1	1	0	1	1	1	
1	1	1	1	1	0	0	0	
1	1	1	1	1	0	0	1	
1	1	1	1	1	0	1	0	
1	1	1	1	1	0	1	1	
1	1	1	1	1	1	0	0	
1	1	1	1	1	1	0	1	
1	1	1	1	1	1	1	0	
1	1	1	1	1	1	1	1	
0	0	0	0	0	0	0	0	Active line time begins

Note: The states of counter D4-D5 from the line-start pulse (LP) to the beginning of the active line time, showing the derivation of control pulses for multiplexers D14-D17 from the fourth and fifth least significant bits (LSB's) and the first-in, first-out buffer memory (FIFO) "shift in" clock from the third least significant bit. MSB = most significant bit.

Figure 11 shows the timing of the first dozen lines after the FP when the frame code is read and entered into the FIFO. Negative edges of the LP signal correspond to beginnings of lines. Active line times begin 9.53 μs later. The leading edge of the FP signal occurs at the same time as a trailing edge of an LP signal; since the clear input to the line counter D35, D36, D37 takes precedence over the clock input, the counter is set to 0. During the recording of the video tape, the frames are numbered in binary, black being 0 and white being 1. During playback, the frame numbers are read into a register as described previously and are available at the ends of lines 0, 1, and 2. In this unit, the first copy of the frame number is ignored; the second and third copies are used. The FP signal is used to set flip-flop D41 (11, 12, 9, 10) so that the 2:1 multiplexer enables the path from the frame code input to the data registers. Because the frame code is 16 bits and the data registers are only 8 bits, the data registers must be strobed in pairs to read frame numbers. At the beginning of line 2,

the frame code developed during line 1 is strobed into registers 1 and 2; at the beginning of line 3, the frame code developed during line 2 is strobed into registers 3 and 4. At the beginning of line 4, the 2:1 multiplexer switches the data path from the frame code input to the data counter, and the contents of the data registers are read into the FIFO. Nothing further happens until line 11, when the first datum arrives. Lines 11 to 252 have data. Nothing is read during lines 253 to 273, these being within the vertical blanking interval between field 1 and field 2. Lines 274 to 516 have data. Lines having data are all read by use of the line cycle described previously.

Each frame of the television signal has 482 lines containing data; each line containing data gives rise to four 8-bit words—1928 words (8-bit bytes) of data per frame. In addition, two copies of the frame code required four 8-bit bytes. That there are 30 frames every second implies that the data rate is 57,960 bytes per second. The Interdata 7/32 computer can accept data at this rate if the machine is operated in the burst mode. The computer is programed to read nine bursts of 200 words and one burst of 132 words for each frame. The machine indicates that it has read a particular data byte, and this signal is used to advance the FIFO one byte.

Up to this point, only normal operation has been considered. Two abnormal conditions are caused by anomalies in the VTR and by starting all the equipment: VTR frame, decoder, Video Processor, and Digitizer/Interface. These conditions are handled in a surprisingly similar way. From the discussion of the way that the data are presented to the computer, it is seen that serious difficulty occurs only if a group of 1932 bytes of data does not correspond to exactly one frame. If 525 LP's occur after an FP, then the Digitizer/Interface enters 1932 bytes of data into the FIFO. The content of the data registers being wrong is an error dealt with during subsequent processing. The only error that requires dropping the entire frame is the lack of 525 lines between FP's. This error is indicated on a status line to the computer (SIN070); if an error occurs, the computer ignores the frame and awaits the next frame. Initial sync of the entire system is accomplished in the same way. The entire system is turned on, and then the tape recorder is started. While the tape is coming up to speed, many frames do not have the proper number of lines. During this period, the Digitizer/Interface indicates many errors and, consequently, the computer does not take any data. After the tape speed has stabilized, no more errors are detected, and the machine goes along on its merry way.

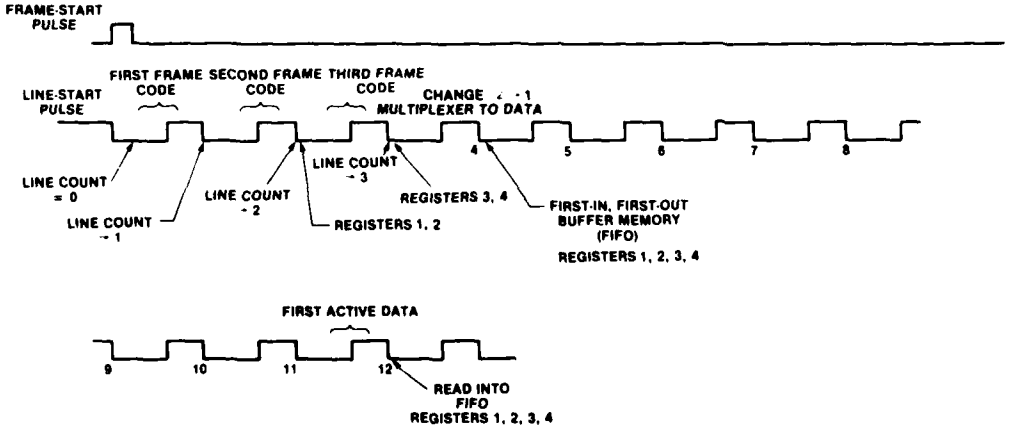


Figure 11. Details of timing at beginning of frame.

If the ultimate destination of the digital data were the core memory of the Interdata 7/32, then the system described so far would provide satisfactory results. However, the maximum number of frames that can be held in the core is approximately 25, and a typical cloud experiment lasts several minutes and involves thousands of frames. Therefore, the ultimate destination of the data must be a mass storage medium—in our case, a floating-head disc. The maximum transfer rate of such a device is quite impressive—several megabytes per second. The key issue in a buffer scheme to a disc, however, is the latency time, which is about 189 ms. It was necessary to match the overall data rate to the overall transfer rate of the disc. Since detecting frame codes modulo 8 is rather simple and since an eightfold reduction in overall data rate was adequate, it was decided that reducing the data via eight passes over the tape was the optimum solution to the average transfer rate problem.

To this end, circuitry to start and stop the digitizer clock was implemented. The 4:16 line decoder, D95, is connected to decode frame numbers that are equal modulo 8 at each of its outputs. After being routed through an eight-position switch, the one-of-eight signal is used to enable flip-flop D90, which is used to control the digitizer clock. D90 is reset by a signal derived from the output of the computer. After each eighth frame, the Interdata 7/32 issues the command to stop the clock and incidently clears the FIFO.

Another signal defect occasioned during head switching is that resulting from incorrect tape tension.[7] The mechanical effect of incorrect tape tension is that when the change is made from one field (and head) to the next, the head just beginning to traverse the tape does so at the correct velocity, but with an error in position. The electrical result of this is a step change in the phase of the recovered line sync pulse train. Naturally, any oscillator locked to this pulse train is momentarily thrown out of lock. In a visual display, the top of the picture is bent to the left or right depending on the sign of the error—hence the expression "skew." In the instrument described in this report, the effect is to unlock the PLL supplying the clock for frame code recovery in just the same manner as do the head-switching transients and therefore similarly to impair the recovery of frame numbers. Nor is the identification of this problem straightforward: until a system has been freed from troubles arising from the head-switching transients, it is indeed difficult to determine that a tape tension problem exists.

Unfortunately, errors in tension are not merely the result of maladjustment of the VTR, although such maladjustment certainly can be troublesome. Tape length is a function of temperature and relative humidity so that tapes made under uncontrolled field conditions may exhibit very substantial step phase error when played back in the laboratory.

4. CONCLUSIONS

At this writing, it is evident that the design is successful: actual data from taped field tests have been obtained in digital form.[8,9] (Early data revealed that the persistence of the written traces on the target of the R7912 scan-converter tube was far too long. A modification to decrease this persistence is given in app B.) It is interesting that some of these field tests were performed not in the air on clouds, but upon the ground on dust and smoke, in an environment physically hostile to instruments and

[7] *Thorsten P Cook, An Automatic Skew Corrector for Helical-Scan Cassette Video Tape Players, J Soc Motion Pict Telev Eng* **82** *(April 1973), 287-289*

[8] *Z G Sztankay, Measurement of the Localized Optical Characteristics of Natural Aerosols, Smoke, and Dust (U), Proceedings of Smoke Symposium II, DRCPM-SMK T-004 78 (June 1978) (CONFIDENTIAL)*

[9] *Z G Sztankay, J Nemarich, J Griffin, W Hattery, and G Wetzel, Backscatter and Extinction Measurements of Smoke Week 2 (U), Proceedings of Smoke/Obscurants Symposium III, DRCPM-SMK T-002 79 (June 1979) (CONFIDENTIAL)*

with the additional problems that result from using ac power sources of low quality and reliability. For example, a corollary experiment depending on an arc lamp was ruined on one occasion by interruption of the power because the arc-striking circuit could not be actuated remotely. Extremes of temperature were encountered. Tapes made under such conditions are necessarily poor, yet even tapes yielding badly torn pictures when displayed could be reduced successfully.

Manifestly the use of this instrument is not limited to the experiment for which it was designed. The relatively high refresh rate and the vast number of data that can be gathered and stored should prove attractive in many applications requiring the acquisition of fast signals under field conditions.

LITERATURE CITED

(1) J. Vanderwall, W. V. Hattery, and Z. G. Sztankay, Subnanosecond Rise Time Pulses from Injection Lasers, IEEE J. Quantum Electron., **QE-10** (July 1974), 570-572.

(2) Z. G. Sztankay and D. W. McGuire, Backscatter in Clouds at 0.9 μm and Its Effect on Optical Fuzing Systems (U), Proceedings of Seventh DoD Conference on Laser Technology (November 1977). (SECRET)

(3) Dennis McGuire, Michael Conner, and Theodore Hopp, Aerosol Discrimination by Electronic High- and Low-Pass Filtering, Harry Diamond Laboratories HDL-TR-1939 (December 1980).

(4) Dennis McGuire and Michael Conner, The Deconvolution of Aerosol Backscattered Optical Pulses to Obtain System-Independent *Aerosol Signatures*, *Harry Diamond* Laboratories HDL-TR-1944 (June 1981).

(5) Yoshio Sawaji, *EIAJ Standards for 1/2* Inch Videotape Recorders, J. Soc. Motion Pict. Telev. Eng., **79** (December 1970), 1091-1093.

(6) Koichi Sadashige, The Effect of the Choice of Tape Format on Broadcast Video Recording, IEEE Broadcasting, **BC-20** (March 1974), 12-16.

(7) Thorsten P. Cook, An Automatic Skew Corrector for Helical-Scan Cassette Video Tape Players, J. Soc. Motion Pict. Telev. Eng., **82** (April 1973), 287-289.

(8) Z. G. Sztankay, Measurement of the Localized Optical Characteristics of Natural Aerosols, Smoke, and Dust (U), Proceedings of Smoke Symposium II, DRCPM-SMK-T-004-78 (June 1978). (CONFIDENTIAL)

(9) Z. G. Sztankay, J. Nemarich, J. Griffin, W. Hattery, and G. Wetzel, Backscatter and Extinction Measurements of Smoke Week 2 (U) Proceedings of Smoke/Obscurants Symposium III, DRCPM-SMK-T-002-79 (June 1979). (CONFIDENTIAL)

APPENDIX A.—MODIFICATION OF TELEVISION READOUT SWEEPS OF TEKTRONIX R7912 TRANSIENT DIGITIZER

Vital to the success of the Video Digitizer and Computer Interface Unit is the interchange of the direction of the scan of the readout of the Tektronix R7912 Transient Digitizer target. This is a particularly easy modification because, at the input to the PARAPHASE AND SCAN AMPLIFIERS, the two ramps are equal in amplitude. The interested reader should consult schematics 5, 6, and 7 of the R7912 maintenance manual[1] for the following description.

Note at the left-hand side of schematic 8, PARAPHASE AND SCAN AMPLIFIERS, the Y ramp is applied to R1000 and the X ramp is applied to R1050 and that at this point both ramps are equal in amplitude, at 10 V. At the deflection plates, however, these amplitudes are in the ratio of 4:3, the standard television aspect ratio. Were the gain adjustment ranges sufficiently great, it would be feasible simply to interchange the deflection plate connections and readjust R1001 and R1051. The range, however, is not great enough, and the modification should be carried out as follows:

(1) On X and Y RAMP GENERATOR BOARD A10, break the Y RAMP line to R1000, break the X RAMP line to R1050, and connect X RAMP to R1000 and Y RAMP to R1050.

(2) On the same board, interchange P515 and P366 to make a similar transposition of the shading circuit.

(3) On SCAN AMPLIFIER BOARD A11, interchange P1119 and P1139.

(4) Adjust the X and Y rotation and centering controls to align the graticule with the television blanking as displayed on a pulse-cross monitor display. These controls are R1097, R1047, R1054, and R1004, respectively, and are found on X and Y RAMP GENERATOR BOARD A10.

This yields a television display with time increasing downward and signal increasing rightward. A scaling factor is introduced (this is apparent when displaying graticule) of 4/3 in amplitude and 3/4 in time. However, the entire target is still read out.

[1] *Tektronix R7912 Transient Digitizer Service Instruction Manual, Tektronix, Inc., Beaverton, OR, 070-1590-00 (August 1976).*

APPENDIX B.—DECREASING LAG IN THE SCAN-CONVERTER TUBE OF THE TEKTRONIX R7912 TRANSIENT DIGITIZER

The solitary method of erasure of the information stored on the target of the scan-converter tube of the Tektronix R7912 is that of scanning it all over by the reading beam. This erasure may be incomplete, depending on the amount of charge that must be transferred (that is, what has been written) and the amount that can be transferred within a given time. (The read gun cathode current divides between the target where it accomplishes the readout-erasure function and the postdeflection mesh where it accomplishes nothing.) Normally, the cathode and the target are only about 10 V apart and, as the read beam acts upon the target, charging its anodes toward the tube cathode potential, more electrons are collected by the mesh. Thus, the efficiency of reading a pixel decreases as the pixel is read.

The unfortunate result is that, at high writing rates and intensities, the target may hold sufficient charge to affect frames other than the frame in which the trace was written. Data have been seen to persist for eight full frames. The difficulty can be greatly alleviated, if not actually eliminated, by raising the target potential and, thus, increasing the reading efficiency. A target-cathode potential of 30 V is considered permissible by the maker. The signal-to-noise ratio may be degraded through increased dark current, but this degradation appears to have no consequence. We have determined by experiment that raising the target-cathode potential from 9 to about 21 V produces an extraordinary reduction in lag—perhaps a tenfold reduction. The modification procedure is given in this appendix.

(1) Referring to pullout schematic 8, READING GUN AND PREAMP, of R7912 Transient Digitizer Interim Instruction Manual,[1] it can be seen that the target potential is established by divider network R1951-R1952. Break the connection of R1951 to the +15 V supply, reconnect it to the +50 V supply, and set R1952 to maximum.

(2) To accommodate the increased target potential, the read beam current should be increased. On the same schematic, note the cathode current adjustment R1893. Maximize the voltage across the test points IK-IK' by adjusting R1893. This maximization raises the cathode current about 60 percent from its nominal value of 750 μA.

(3) Lastly, the Schmitt trigger of the VIDEO PROCESSOR, pullout schematic 9, must be reset to accommodate the increased signal from the preamplifier. The correct level should be determined by experiment. Our experience may be helpful as a guide: the voltage at the slider of R2266 ("DC SCHMITT") was originally +7.1 V. Satisfactory performance was attained with the readjustment of R2266 to produce +1.9 V at this point.

An ineluctable effect of this modification is that the information from field 2 of a frame is degraded. It would be ideal if written data could be made to persist for exactly one frame and then vanish completely. This ideal, however, cannot be reached, so increasing the reading efficiency in the manner described entails at worst the deliberate sacrifice of field 2 of each frame, halving the time resolution. Although this casting away of information is undesirable per se, it proved to be of no importance to the project.

[1] *R7912 Transient Digitizer Interim Instruction Manual, Tektronix, Inc., Beaverton, OR.*

DISTRIBUTION

ADMINISTRATOR
DEFENSE TECHNICAL INFORMATION CENTER
ATTN DTIC-DDA (12 COPIES)
CAMERON STATION, BUILDING 5
ALEXANDRIA, VA 22314

COMMANDER
US ARMY RSCH & STD GP (EUR)
ATTN CHIEF, PHYSICS & MATH BRANCH
FPO NEW YORK 09510

COMMANDER
US ARMY ARMAMENT MATERIEL
READINESS COMMAND
ATTN DRSAR-LEP-L, TECHNICAL LIBRARY
ATTN DRSAR-ASF, FUZE & MUNITIONS
SUPPORT DIVISION
ROCK ISLAND, IL 61299

COMMANDER
US ARMY MISSILE & MUNITIONS
CENTER & SCHOOL
ATTN ATSK-CTD-F
REDSTONE ARSENAL, AL 35809

DIRECTOR
US ARMY MATERIEL SYSTEMS ANALYSIS ACTIVITY
ATTN DRXSY-MP
ABERDEEN PROVING GROUND, MD 21005

DIRECTOR
US ARMY BALLISTIC RESEARCH LABORATORY
ATTN DRDAR-TSB-S (STINFO)
ABERDEEN PROVING GROUND, MD 21005

TELEDYNE BROWN ENGINEERING
CUMMINGS RESEARCH PARK
ATTN DR. MELVIN L. PRICE, MS-44
HUNTSVILLE, AL 35807

ENGINEERING SOCIETIES LIBRARY
ATTN ACQUISITIONS DEPARTMENT
345 E. 47TH STREET
NEW YORK, NY 10017

HQ, USAF/SAMI
WASHINGTON, DC 20330

US ARMY ELECTRONICS TECHNOLOGY
& DEVICES LABORATORY
ATTN DELET-DD
FT MONMOUTH, NJ 07703

COMMANDER
US ARMY ARMAMENT RESEARCH
& DEVELOPMENT COMMAND
ATTN DRDAR-SE, SYSTEMS EVALUATION
OFFICE, LTC GRADY COOK
DOVER, NJ 07801

US ARMY ELECTRONICS RESEARCH
& DEVELOPMENT COMMAND
ATTN TECHNICAL DIRECTOR, DRDEL-CT

HARRY DIAMOND LABORATORIES
ATTN CO/TD/TSO/DIVISION DIRECTORS
ATTN RECORD COPY, 81200
ATTN HDL LIBRARY, 81100 (2 COPIES)
ATTN HDL LIBRARY, 81100 (WOODBRIDGE)
ATTN TECHNICAL REPORTS BRANCH, 81300
ATTN CHAIRMAN, EDITORIAL COMMITTEE
ATTN LEGAL OFFICE, 97000
ATTN CHIEF, 13000
ATTN CHIEF, 11000
ATTN CHIEF, 13300 (15 COPIES)
ATTN CHIEF, 11400
ATTN MORRISON, R., 13500 (GIDEP)
ATTN COX, L., 00211
ATTN HUMPHREY, R., 13300
ATTN GRIFFIN, J. R., 21100
ATTN HATTERY, W. V., 13300
ATTN SANN, K. H., 15000
ATTN PEPERONE, S., 42600
ATTN DOBRIANSKY, B., 13500 (2 COPIES)
ATTN LANHAM, C., 00213
ATTN GIGLIO, D., 15300
ATTN GEIPE, T., 22100
ATTN LAMB, R., 22900
ATTN TUTTLE, J., 21400
ATTN MCGUIRE, D., 13300
ATTN VANDERWALL, J., 22800 (10 COPIES)
ATTN CONNER, M., 15200 (10 COPIES)


FILMED
5-8